35. (New) A device according to claim 19, wherein edges of said insulating film in said contact hole are rounded off.

36. (New) A device according to claim 19, further comprising an electrode connected with one of said source and drain regions through said contact hole.

37. (New) A device according to claim 24, wherein edges of said insulating film in said contact hole are rounded off.--

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

By this amendment, claims 1, 2, 6, 10, 11, 14, 16, 19, and 24 are amended, and new claims 31-37 are added. Many of the claims now define an electrode connected with one of the source and drain regions through first, second, and third openings. This subject matter is shown in FIGs. 2D and 8B. Claims 1 and 3-5 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Fu. The rejection asserts that Fu shows a semiconductor device with an insulating film of SiO_2 over a semiconductor layer. Two different silicon nitride interlayer insulating films are formed on the SiO_2 film. A contact hole

with tapered sides is formed through the SiO_2 insulating film and two SiN interlayer insulating films.

It should be noted, however, that Fu does not teach the claimed aspect whereby edges of at least the third opening are rounded off as defined by claims 1, 6, 19, and 24. This is supported by FIGs. 2D, 4, and 8B. This aspect enables coverage of electrodes in the contact hole to be improved. Moreover, poor contact in and around the contact holes in the semiconductor device can be eliminated.

Claims 2 and 6-18 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Fu in view of Auda. Claims 19-30 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fu in view of Auda and Huang. The rejection asserts that Fu shows many aspects of the invention and that Auda shows a tapered angle of the second interlayer insulating film in the contact hole is larger than the tapered angle of the first insulating film in the contact hole. Huang is cited to show that low doped impurity region are may be located in a semiconductor layer.

It should be noted, however, that Auda's FIG. 1C as cited shows the halfway point in a process of forming the contact hole. The final opening is shown in FIG. 1D. A tapered angle A of the overlayer insulating film 12B of PGS in the contact hole appears to be the same as the tapered angle A of the underlayer

insulating film 12A of SiO_2. There would appear to be no reason to combine Fu's device with the interim contact hole described by Auda. In fact, Auda never teaches using this interim structure in FIG. 1C as it is. Auda express teaching is that the contact hole should prior to its use.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 8/6/01

Scott C. Harris
Reg. No. 32,030

SCH/smr

Fish & Richardson P.C.
PTO Customer No. 20985
4350 La Jolla Village Drive, Suite 500
San Diego, CA 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

10126444.doc

VERSION TO SHOW CHANGES MADE

Claims 1, 2, 6, 10, 11, 14, 16, 19, and 24 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor layer having at least channel, source and drain regions;

an insulating film formed on said semiconductor layer

a first interlayer insulating film over said insulating film;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said insulating film and a portion of said first interlayer insulating film where surrounds said second opening,

wherein edges of at least said [first and] third opening[s] are rounded off.

2. (Amended) A device according to claim 1 wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor layer in the second opening.

6. (Amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface, said semiconductor layer having at least channel, source and drain regions;

a gate insulating film over said semiconductor layer;

a first interlayer insulating film over said gate insulating layer;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said gate insulating film;

a first opening in said gate insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said gate insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said gate insulating film and a portion of said first interlayer insulating film where surrounds said second opening,

wherein edges of at least said [first and] third opening[s] are rounded off, and

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor layer in the second opening.

10. (Amended) A semiconductor device comprising:

a semiconductor layer having at least channel, source and drain regions;

an insulating film on said semiconductor layer

a first interlayer insulating film over said insulating film;

a second interlayer insulating film on said first interlayer insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film where surrounds said first opening; [and]

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said insulating film and a portion of said first interlayer insulating film where surrounds said second opening; and

an electrode formed on said first, second, and third openings and connected with one of said source and drain regions through said first, second, and third openings,

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to a major surface of said semiconductor layer in the second opening.

11. (Amended) A device according to claim 10, wherein said [gate] insulating film comprises silicon oxide.

14. (Amended) A semiconductor device comprising:

a semiconductor layer including at least channel, source and drain regions;

an insulating film on said semiconductor layer

multi-interlayer insulating films comprising at least an upper insulating layer and a lower insulating layer over said insulating film, said lower insulating layer comprising the same material as said upper insulating layer; [and]

at least one contact hole in said multi-interlayer insulating films and said insulating film, said contact hole having a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein a taper angle β of an inner surface of the upper insulating layer in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of the lower insulating layer in the contact hole with respect to said major surface of said semiconductor layer.

16. (Amended) A device according to claim 14, wherein said [first and second interlayer insulating films] lower and upper insulating layers comprise a material selected from the group consisting of silicon nitride and organic resin.

19. (Amended) A semiconductor device comprising:

a semiconductor layer having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

an interlayer insulating film [consisting of] comprising a plurality of insulating layers over said semiconductor layer and said [first interlayer] insulating film; and

a contact hole in said interlayer insulating film and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section,

wherein edges of [said insulating film and] said interlayer insulating film in said contact hole are rounded off, and

wherein angles of the tapered section of the contact hole decrease successively from a top interlayer insulating layer toward a bottom interlayer insulating layer.

24. (Amended) A semiconductor device comprising:

a semiconductor layer having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said

channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

an interlayer insulating film [consisting of] comprising a plurality of insulating layers over said semiconductor layer and said [first interlayer] insulating film; and

a contact hole in said interlayer insulating film and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein edges of [said insulating film and] said interlayer insulating film in said contact hole are rounded off[, and

wherein said portion of said high doped impurity region is apart from a junction between said low and high doped impurity regions].